

CLAIMS

What is claimed is:

- 1 1. A system which indicates semiconductor device fabrication defects
2 comprising:
3 test data corresponding to testing of a plurality of fuses, each one of the
4 plurality of fuses residing on a different one of a plurality of semiconductor devices
5 and each one of the plurality of fuses having a common location on the semiconductor
6 devices; and
7 a memory with logic configured to determine from the test data which of the
8 plurality of fuses are defective fuses, and further configured to specify on an output
9 report the common location of the determined defective fuses when a number of the
10 defective fuses are at least equal to a predefined portion of the plurality of fuses.
- 1 2. The system of claim 1, further comprising a fuse test device configured
2 to test the plurality of fuses.
- 1 3. The system of claim 2, wherein the fuse test device further comprises a
2 fuse test unit configured to test the plurality of fuses when the semiconductor device
3 resides on a wafer.
- 1 4. The system of claim 2, wherein the fuse test device further comprises a
2 fuse test unit configured to test the plurality of fuses when the semiconductor device
3 resides on a die.
- 1 5. The system of claim 2, wherein the fuse test device further comprises a
2 fuse test unit configured to test the plurality of fuses when the semiconductor device
3 resides on an integrated circuit chip.

1 6. The system of claim 2, wherein the fuse test device further comprises a
2 fuse test unit configured to test the plurality of fuses when the semiconductor device
3 resides on a circuit board.

1 7. A method for indicating semiconductor device fabrication defects, the
2 method comprising:
3 retrieving test data corresponding to test results from a plurality of fuses, each
4 one of the plurality of fuses residing on a different one of a plurality of semiconductor
5 devices and each one of the plurality of fuses having a common location on the
6 semiconductor devices;
7 determining from the test data which of the plurality of fuses are defective
8 fuses; and
9 specifying on an output report the common location of the determined
10 defective fuses when a number of the defective fuses are at least equal to a predefined
11 portion of the plurality of fuses.

1 8. The method of claim 7, further comprising specifying the predefined
2 portion as a percentage.

1 9. The method of claim 7, further comprising:
2 retrieving the test data corresponding to the test results from a plurality of
3 second fuses, each one of the plurality of second fuses residing on a different one of
4 the semiconductor devices and each one of the plurality of second fuses having a
5 second common location on the semiconductor devices;
6 determining from the test data which of the plurality of second fuses are
7 defective second fuses; and
8 specifying on the output report the second common location of the determined
9 defective second fuses when a number of the defective second fuses are at least equal
10 to the predefined portion of the plurality of second fuses.

1 10. The method of claim 7, further comprising:
2 retrieving the test data corresponding to the test results from a plurality of fuse
3 arrays, each one of the fuse arrays having a plurality of array fuses and each one of the
4 plurality of fuse arrays having a common fuse array location on the semiconductor
5 devices;
6 determining from the test data which of the plurality of array fuses are
7 defective array fuses; and
8 specifying on the output report the common fuse array location when a number
9 of the defective array fuses are at least equal to a predefined portion of the array fuses.

1 11. The method of claim 7, further comprising:
2 retrieving the test data corresponding to the test results from a plurality of fuse
3 registers, each one of the fuse registers having a plurality of register fuses and each
4 one of the plurality of fuse registers having a common fuse register location on the
5 semiconductor devices;
6 determining from the test data which of the plurality of register fuses are
7 defective register fuses; and
8 specifying on the output report the common fuse registers location when a
9 number of the defective register fuses are at least equal to a predefined portion of the
10 register fuses.

1 12. The method of claim 7, further comprising:
2 retrieving the test data corresponding to the test results from a grouping of
3 fuses, each one of the grouped fuses in the grouping of fuses having a common
4 location on the semiconductor devices;
5 determining from the test data which of the grouped fuses are defective; and
6 specifying on the output report the common location when a number of the
7 defective grouped fuses are at least equal to a predefined portion of the grouped fuses.

1 13. The method of claim 7, further comprising displaying the output report.

1 14. The method of claim 7, further comprising printing the output report.

1 15. The method of claim 7, further comprising testing the plurality of
2 fuses.

1 16. A system for identifying semiconductor device fabrication defects,
2 comprising:

3 means for retrieving test data corresponding to test results from a plurality of
4 fuses, each one of the plurality of fuses residing on a different one of a plurality of
5 semiconductor devices and each one of the plurality of fuses having a common
6 location on the semiconductor devices;

7 means for determining from the test data which of the plurality of fuses are
8 defective fuses;

9 means for generating an output report the common location of the determined
10 defective fuses when a number of the defective fuses are at least equal to a predefined
11 portion of the plurality of fuses; and

12 means for displaying the output report.

1 17. The system of claim 16, further comprising:

2 means for retrieving the test data corresponding to the test results from a
3 plurality of second fuses, each one of the plurality of second fuses residing on a
4 different one of the semiconductor devices and each one of the plurality of second
5 fuses having a second common location on the semiconductor devices;

6 means for determining from the test data which of the plurality of second fuses
7 are defective second fuses; and

8 means for specifying on the output report the second common location of the
9 determined defective second fuses when a number of the defective second fuses are at
10 least equal to the predefined portion of the plurality of second fuses.

1 18. The system of claim 16, further comprising:
2 means for retrieving the test data corresponding to the test results from a
3 plurality of fuse arrays, each one of the fuse arrays having a plurality of array fuses
4 and each one of the plurality of fuse arrays having a common fuse array location on
5 the semiconductor devices;
6 means for determining from the test data which of the plurality of array fuses
7 are defective array fuses; and
8 means for specifying on the output report the common fuse array location
9 when a number of the defective array fuses are at least equal to a predefined portion of
10 the array fuses.

1 19. The system of claim 16, further comprising:
2 means for retrieving the test data corresponding to the test results from a
3 plurality of fuse registers, each one of the fuse registers having a plurality of register
4 fuses and each one of the plurality of fuse registers having a common fuse register
5 location on the semiconductor devices;
6 means for determining from the test data which of the plurality of register
7 fuses are defective register fuses; and
8 means for specifying on the output report the common fuse register location
9 when a number of the defective register fuses are at least equal to a predefined portion
10 of the register fuses.

1 20. The system of claim 16, further comprising:
2 means for retrieving the test data corresponding to the test results from a
3 grouping of fuses, each one of the grouped fuses in the grouping of fuses having a
4 common location on the semiconductor devices;
5 means for determining from the test data which of the plurality of grouped
6 fuses are defective; and
7 means for specifying on the output report the common location when a number
8 of the defective grouped fuses are at least equal to a predefined portion of the grouped
9 fuses.

1 21. A computer-readable medium having a program for indicating
2 semiconductor device fabrication defects, the program comprising logic configured to
3 perform:
4 receiving from a memory test data corresponding to test results from a
5 plurality of fuses, each one of the plurality of fuses residing on a different one of a
6 plurality of semiconductor devices and each one of the plurality of fuses having a
7 common location on the semiconductor devices;
8 determining from the test data which of the plurality of fuses are defective
9 fuses; and
10 specifying on an output report the common location of the determined
11 defective fuses when a number of the defective fuses are at least equal to a predefined
12 portion of the plurality of fuses.